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(54) Improvements in or relating to intergrated circuits

(57) A thick plated interconnect (80) comprising a copper lead (50) and a bonding cap (84) coupled to the copper lead (50). The bonding cap (84) may include a bondable member (86) formed from a bondable layer (62) comprising aluminum. A barrier member (88) may be formed from a barrier layer (60). The barrier member (88) may be disposed between the bondable member (86) and the copper lead (50).

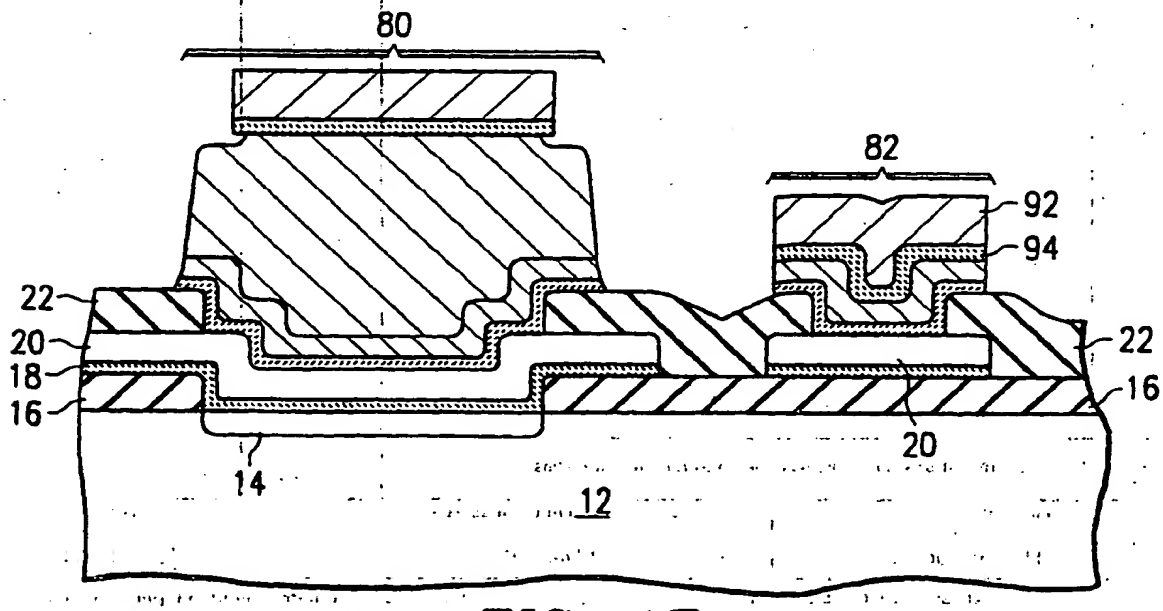

FIG. 1E

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Description

TECHNICAL FIELD OF THE INVENTION

The present invention relates generally to the field of integrated circuits, and more particularly to an improved thick plated interconnect and to an associated auxiliary interconnect for an integrated circuit.

BACKGROUND OF THE INVENTION

Thick plated metal interconnects can be used to provide low resistance pathways in integrated circuits. The interconnects may be employed for high current bussing and similar applications of power integrated circuits and other types of integrated circuits. The interconnects may be in the form of copper because of its low resistance.

Bonding directly to copper interconnects would enhance the performance of integrated circuits by eliminating the high parasitic series resistance associated with bond pads and standard multi-level VLSI metal systems. Typical bonding systems such as aluminum wedge and gold ball bonding, however, suffer reliability problems when bonded to copper due to voiding of aluminum in copper. Copper on copper bonds also suffer reliability problems.

To overcome such reliability problems, nickel plating has been used as a cap metalization system for thick plated copper interconnects. Although a nickel cap has been demonstrated to work reliably for large aluminum wedge bonding, its manufacturability is not standard and its environmental cleanup is costly, and it is not reliable for gold bonds.

SUMMARY OF THE INVENTION

Accordingly, a need has arisen in the art for an improved thick plated metal interconnect. The present invention provides a thick plated interconnect having an aluminum bonding cap that substantially eliminates or reduces the disadvantages and problems associated with prior thick plated interconnects.

In accordance with the present invention, a thick plated interconnect may comprise a copper lead and a bonding cap coupled to the copper lead. The bonding cap may include a bondable member formed from a bondable layer comprising aluminum. A barrier member may be formed from a barrier layer. The barrier member may be disposed between the bondable member and the copper lead.

More specifically, in one embodiment, the thick plated interconnect may include a section of a copper seed layer. In this embodiment, the copper lead may be plated to the section of the copper seed layer. The bondable layer may comprise an aluminum alloy including silicon and copper. In a specific embodiment, the aluminum alloy may include about one (1) percent silicon and about one-half (0.5) percent copper.

In accordance with another aspect of the present invention, an auxiliary interconnect may comprise a second section of the copper seed layer. An auxiliary bonding cap may be coupled to the second section of the copper seed layer. The auxiliary bonding cap may include an auxiliary member formed from the bondable layer. An auxiliary barrier member may be formed from the barrier layer. The auxiliary barrier member may b disposed between the auxiliary bondable member and the second section of the copper seed layer.

Important technical advantages of the present invention include providing a thick plated interconnect that substantially reduces or eliminates bonding resistance. In particular, a bonding cap capable of receiving conventional gold wire and aluminum wedge bonds may be formed on a copper lead. Accordingly, bonds may be formed directly on the thick plated interconnect and high parasitic series resistance associated with bond pads is eliminated.

Another technical advantage of the present invention includes providing an auxiliary interconnect formed from some of the same layers of the thick plated interconnect including the bond cap, seed and barrier layers and without additional processing steps. In particular, the auxiliary interconnect may be formed at any location common to fabrication steps of the thick plated interconnect and used where the very low resistance of copper plating is not required. The auxiliary interconnect provides more interconnect flexibility by providing a free level of interconnect. Additionally, the auxiliary interconnect provides a relatively small and low resistance interconnect that allows denser circuit designs resulting in die area savings.

Still another technical advantage of the present invention includes providing an improved mold for plating the copper lead of the thick plated interconnect. In particular, the mold may include a cavity formed in a photoresist layer exposing a section of a copper seed layer electrically coupled to an underlying metal layer through a via in a dielectric layer. A barrier layer may be disposed between a copper seed layer and the underlying metal layer.

Other technical advantages will be readily apparent to one skilled in the art from the following figures, d - scriptions, and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and its advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings, wherein like reference numerals represent like parts, in which:

FIGURES 1A-E are a series of schematic cross-sectional diagrams illustrating a method of fabricating an improved thick plated copper interconnect and associated auxiliary metal interconnect in accordance with

one embodiment of th present invention.

DETAILED DESCRIPTION OF THE INVENTION

The preferred embodiments of the present invention and its advantages are b st understood by referring now in more detail to FIGURES 1A-E of the drawings, in which like numerals refer to like parts throughout the several views. FIGURES 1A-E illustrate a method of fabricating a copper plated interconnect having an aluminum bonding cap and an associated auxiliary interconnect in accordance with one embodiment of the present invention. As described in more detail below, the aluminum bonding cap allows direct bonding to the interconnect for low resistance applications. The auxiliary interconnect is formed with the interconnect and without additional processing steps.

FIGURE 1A illustrates an initial semiconductor structure 10. The initial semiconductor structure 10 may comprise a semiconductor layer 12 including an integrated circuit having one or more interlevel contacts 14. The semiconductor layer 12 may be a substrate such as a wafer. It will be understood that the semiconductor layer 12 may also be a layer of semiconductor material formed on a substrate. For example, the semiconductor layer 12 may be an epitaxial layer grown on a wafer. It will be understood that the layer 12 may also be another system of interconnects such as another layer of metal or multiple layers of metal with appropriate isolation layers as the process dictates. Here is shown as an exemplary single metal system for simplicity.

An interlevel oxide 16, barrier layer 18, metal layer 20, and dielectric layer 22 may be formed on the semiconductor layer 12. The interlevel oxide 16 isolates the integrated circuit of the semiconductor layer 12 generally from the barrier layer 18. The interlevel oxide 16 may be patterned and etched to allow the barrier layer 18 to contact the integrated circuit of the semiconductor layer 12 at the interlevel contact 14. The metal layer 20 is a top surface conventional metal layer associated with the process such as for a double level metal layer or for a triple level metal layer. Accordingly, it will be understood that a present invention is not limited to use with a single level system, but may include multi-level interconnect systems.

The barrier layer 18 provides both an electrical contact and a mechanical barrier between the interlevel contact 14 of the semiconductor layer 12 and the metal layer 20. Accordingly, the barrier layer 18 allows current to flow between layers while preventing voiding and similar types of mechanical problems. The barrier layer 18 may comprise any conductor that does not adversely react with the interlevel contact of the semiconductor layer 12 or the metal layer 20.

The dielectric layer 22 may be a passivation overcoat isolating the initial semiconductor structure 10 generally from subsequent integrated circuit processing. Dielectric layer 22 may be composed of several layers of dielectric having different ch mical mak up. Dielectric layer 22 may be oxide and nitride or oxide and oxinitrid . The passivation overcoat 22, however, may be patterned and etched to form vias 24 to expose the initial semiconductor structur 10 to subsequent integrat d circuit processing at specific locations. For the embodiment of FIGURE 1A, a via 24 may be formed in the passivation overcoat 22 over the interlevel contact 14 of the semiconductor layer 12. Accordingly, the interlevel contact 14 may be electrically connected to subsequently formed integrated circuit layers through the via 24 by the barrier layer 18 and the metal layer 20. A second via 24 may also be formed in the passivation overcoat 22 for an auxiliary metal system 26. As explained in mor detail below, the auxiliary metal system may form an auxiliary interconnect. The use of the terms "contacts" and "vias" for interconnection of metal and semiconductor systems will be obvious to those skilled in the art.

In one embodiment, the semiconductor layer 12 may comprise silicon and the metal layer 20 may comprise aluminum composition. In this embodiment, th barrier layer 18 may comprise tungsten, titanium tungsten or platinum silicide, which will not react with either the silicon or the aluminum. As previously described, the metal layer 20 may be a system of interconnects including multiple level metal and corresponding barrier metals and polysilicon interconnects. The various metal systems may be isolated by appropriate dielectric layers. The barrier metals may be tungsten, platinum, titanium, and other combinations described above. The connection between metal systems is made by vias whereas connection to the actual silicon circuit is termed "contacts." Generally, the term "vias" is used for connections between interconnects and "contact" is used for connection to silicon or polysilicon. The interlevel oxide 16 may comprise silicon dioxide and the passivation overcoat 22 may comprise a nitride overcoat. It will be understood that the semiconductor layer 12, interlevel oxide 16, barrier layer 18, metal layer 20, and passivation overcoat 22 may comprise other materials within the scope of the present invention. For example, the interlevel oxide 16 and passivation overcoat 22 may be formed from other dielectric materials. Additionally, the barrier layer 18 may be any conductor that provides a mechanical barrier between layers. It will be further understood that although the embodiment of FIGURE 1A includes only a single layer of metal, the initial semiconductor structure 10 may comprise multiple metal layers within the scope of the present invention. Thus, as previously described, additional systems of interconnects such as another layer of metal or multiple layers of metal with appropriate isolation layers may be included as the process dictates.

Referring to FIGURE 1B, a barrier lay r 30 may b formed on the surface of the initial semiconductor structure 10. As shown by FIGURE 1B, the barrier layer 30 may contact the metal layer 20 through the vias 24 and elsewhere contact the passivation layer 22. The barrier

layer 30 may protect the underlying metal layer 20 from subsequent metal processes. The barrier layer 30 may also act as an etch stop to protect areas from having the metal layer 20 etched away where the vias 24 exists during subsequent metal etching steps. The barrier layer 30 also protects a layer deposited s ed layer and thick plated layer from contamination from the dielectric and vice versa.

In one embodiment, the barrier layer 30 may be titanium tungsten (TiW). In this embodiment, the titanium tungsten may be sputter deposited onto the initial semiconductor structure 10. It will be understood that the barrier layer 30 may comprise other conductors capable of protecting the underlying metal layer 20 within the scope of the present invention. For example, the barrier layer 30 may comprise a varied metallurgical alloy or the like.

A copper seed layer 32 may be deposited onto the barrier layer 30. Preferably, the copper seed layer 32 comprises copper. It will be understood that the copper seed layer 32 may comprise other materials capable of acting as a seed for copper plating. As described in more detail below, copper will plate to the copper seed layer 32 to form thick copper interconnect.

For the embodiment of FIGURE 1B, a section 34 of the copper seed layer 32 may be in electrical contact with the interlevel contact 14 of the semiconductor layer 12 through the barrier layers 30 and 18 and the metal layer 20. Elsewhere, the copper seed layer 32 may be generally isolated from the semiconductor layer 12 by the passivation layer 22. A second section 36 of the copper seed layer 32 may be in electrical contact with the metal layer 20 through the barrier layer 30 at the auxiliary metal system 26.

In a particular embodiment, the copper seed layer 32 may be sputter deposited on the barrier layer 30. In this embodiment, the copper seed layer 32 may be deposited to a thickness of about 2,000 angstroms. It will be understood that the copper seed layer 32 may be otherwise deposited within the scope of the present invention.

A photoresist layer 40 may be deposited on the copper seed layer 32. The thickness of the photoresist layer 40 is driven by the thickness of the copper plating desired for the copper interconnect. In one embodiment, the photoresist layer 40 may be 12,000 angstroms thick, which will allow up to 11,000 angstroms of copper to be plated. If a greater thickness of copper plating is desired, multiple layers of photoresist may be used.

The photoresist layer 40 may be patterned and etched to form a cavity 42 exposing the section 34 of the copper seed layer 32 electrically coupled to the underlying metal layer 20 through the via 24 in the passivation overcoat 22. Preferably, the photoresist layer 40 is patterned such that the cavity 42 overlaps the section 34 of the copper seed layer 32 by a distance great enough to compensate for misalignment of the pattern and still result in the patterned cavity efficiently overlapping 34a the section 34 of the copper seed layer 32.

As shown by FIGURE 1B, the cavity 42 in the photoresist layer 40 may in conjunction with the cavity and passivation layers 16 and 22 lined by copper seed layer 32 and the barrier metal 30 forming the section 34 form a combination layer mold 44 over the interlevel contact 14. It will be understood that the bombination layer mold 44 may comprise other materials within the scope of the present invention. For example, the photoresist and the passivation material may include combinations of other dielectric materials such as oxide glasses, like silicon dioxide, and/or polymides and/or polysilicons and/or selective epitaxials and/or other materials.

Referring to FIGURE 1C, a copper lead 50 may be plated to the copper seed layer 32 exposed by the cavity 42 in the combination layer mold 44. In one embodiment, the copper lead 50 may be plated by a conventional electroplating process. In this embodiment, the semiconductor device may be disposed in a copper electroplating bath. In the electroplating bath, copper will plate to the copper seed layer 32 exposed in the combination layer mold 44. In one embodiment, as previously described, the copper lead 50 may be plated to a thickness of 11,000 angstroms. It will be understood that the thickness of the copper plating may be varied within the scope of the present invention.

Referring to FIGURE 1D, the photoresist layer 40 may be removed to leave the thick plated copper lead 50. The photoresist layer 40 may be removed by conventional etching techniques. It will be understood that the photoresist layer 40 may be otherwise removed within the scope of the present invention.

As shown by FIGURE 1D, the copper lead 50 may be electrically connected with the interlevel contact 14 of the semiconductor layer 12 through the section 34 of the copper seed layer 32, metal layer 20, and barrier layers 18 and 30. The copper lead 50 will not be in electrical contact with the interlevel contact 14 where the combination layer mold 38 is formed over the passivation overcoat 22. In this case, the copper lead 50 will be electrically isolated from the metal layer 20 and other components of the semiconductor device.

A barrier layer 60 may be formed on the surface of the semiconductor structure 10 by sputtering methods. As shown by FIGURE 1D, the barrier layer 60 may contact the top surface of the copper lead 50 and elsewhere the copper seed layer 32. The barrier layer 60 may protect the underlying copper of the lead 50 and seed layer 32 from subsequent metal processes. The barrier layer 60 may also protect later added materials from interaction with the copper which may cause voiding and other deformities.

In one embodiment, the barrier layer 60 may be sputtered titanium tungsten (TiW). Accordingly, the same metal may be used for both barrier layers 60 and 30. Use of titanium tungsten for both barrier layers 30 and 60 may make the present invention more manufacturable with standard VLSI and ULSI sputter processing

techniques. Specific examples of such process technologies include PRISM, EPIC, LBC, and power plus Arrays.

Th titanium tungsten of the barrier layer 60 may be sputter deposited onto the semiconductor structure. It will be understood that the barrier layer 60 may comprise other conductors capable of preventing copper from reacting with later deposited materials. For example, the barrier layer 60 may comprise a varied metallurgical alloy or the like.

The barrier layers 30 and 60 sandwich the copper lead 50 and copper seed layer 32 such that the copper is not exposed to other metal layers or systems or dielectrics or systems. The barrier layers 30 and 60 may form ridged surfaces against abutting copper surfaces.

A bondable layer 62 may be formed on the barrier layer 60. In one embodiment, the bondable layer 62 may be sputter deposited onto the barrier layer 60. The bondable layer 62 may have a standard thickness of about 0.6 microns. It will be understood that the thickness of the bondable layer 62 may vary depending on the application for the interconnect.

The bondable layer 62 may comprise an aluminum alloy. In one embodiment, the bondable layer 62 may comprise aluminum with 1% silicon and a half percent copper (Al 1%Si 0.5%Cu). This metal may be deposited with conventional sputtering process technology.

A photoresist layer 70 may be formed on the bondable layer 62. The photoresist layer 70 may be deposited in accordance with the conventional photoresist technology. In one embodiment, the photoresist layer 70 may have a thickness of between 0.6 and 1.4 microns. It will be understood that the thickness of the photoresist may vary within the scope of the present invention. The photoresist layer 70 may be patterned and etched to leave photoresist only above bonding and auxiliary interconnect regions 72. Referring to FIGURE 1E, the semiconductor structure may be etched to remove sections of the bondable layer 62, barrier layer 60, copper seed layer 32 and barrier layer 30 not covered by the patterned photoresist layer 70. In one embodiment, the unprotected layers may be removed by an etched sequence applied in a specific order such that unprotected sections of the bondable layer 62 are etched away first, followed by underlying sections of the barrier layer 60 second, copper seed layer 32 third, and barrier layer 30 fourth. Accordingly, the etched sequence may be a top down etch removing the top or uppermost layer first and so on down through the following layers as required. Each etch of the sequence may be a standard chemical etch as prescribed in compatible processing.

Between etching barrier layer 60 and copper seed layer 32, a photoresist reflow may optionally be used to protect the remaining sections of the bondable layer 62 from being etched under edges of the pattern photoresist layer 70. Such undercut etching may occur at the edges of the patterned bondable layer 62 because edges of the remaining section of the bondable layer 62 will be exposed after etching th bondable layer 62 and the barrier layer 60. Reflow of photoresist may cover the exposed edges and help reduce undercutting of the bondable layer 62 during th subs quent etch of the copper seed layer 32. After etching, a nitrid or other mat rial passivation may be deposited and patterned to expose regions to be bonded to.

The patterned photoresist layer 70 may be removed to leave a thick plated copper interconnect 80 and associated auxiliary metal interconnect 82. The thick plated copper interconnect 80 may include a bonding cap 84 directly on top of the copper lead 50. As shown by FIGURE 1E, the bonding cap 84 may comprise a bondable member formed from the bondable layer 86 and a barrier member 88 formed from the barrier layer 30 at the bonding region 72 above the copper lead 50. Accordingly, conventional gold wire and aluminum wedge bonds may be formed directly on the thick plated int r-connect 80. The barrier member 88 prevents voiding of a bond with the copper lead 50. Accordingly, the bonds will not deteriorate and become mechanically or el ctrically unreliable. Accordingly, high parasitic series resistance associated bond pads is eliminated.

The auxiliary interconnect 82 is formed from the bondable layer 62, barrier layer 60, seed layer 32, and the barrier layer 30. The auxiliary interconnect 82 has a property of small geometry line control and the copper seed layer provides excellent electromigration control.

The auxiliary interconnect 82 is associated with the thick plated copper interconnect 80 in that the auxiliary interconnect 82 is formed form some of the layers of the thick plated copper interconnect 80 and without additional processing steps. The auxiliary interconnect 82 may be used where copper plating is not required. Advantageously, the auxiliary interconnect 82 provides interconnect flexibility by providing a free level of interconnect. Additionally, the auxiliary interconnect 82 provides a relatively small and low resistance interconnect that allows denser circuit designs resulting in die area savings.

Although the present invention has been described with several embodiments, various changes in modifications may be suggested to one skilled in the art. It is intended that the present invention accomplish such changes and modifications as fall within the scope of the appended claims.

Claims

1. A plated interconnect having a bonding cap coupled to a copper lead, comprising:

a bondable member formed from a bondable layer comprising aluminum;

a barrier member formed on a barrier layer; and

wherein the barrier member is disposed between the bondable member and the copper

lead.

2. The interconnect of Claim 1, wherein the bondable layer comprises an aluminum alloy comprising silicon and copper.

3. The interconnect of Claim 1 or Claim 2, wherein the bondable layer comprises an aluminum alloy comprising between 1 percent silicon and between 0.5 and 2 percent copper.

4. The interconnect of any of Claims 1 to 3, wherein the bondable layer comprises an aluminum alloy comprising about one (1) percent silicon and about one half (0.5) percent copper.

5. The interconnect of any of Claims 1 to 4, wherein the barrier layer comprises titanium tungsten (TiW).

6. The interconnect of any of Claims 1 to 5, further comprising:

a copper seed layer; and
wherein the copper lead is plated to the copper seed layer.

7. The interconnect of Claim 6, wherein: the copper seed layer is electrically coupled to an underlying metal layer; and
a second barrier layer is disposed between the copper seed layer and the underlying metal layer.

8. The interconnect of Claim 7, wherein the second barrier layer comprises titanium tungsten (TiW).

9. The interconnect of any of Claims 1 to 8, wherein the copper lead comprises a thickness greater than 10,000 angstroms.

10. A semiconductor device, having a plated interconnect, comprising:

a portion of a copper seed layer;
a copper lead plated to the portion of the copper seed layer;
a bonding cap coupled to the copper lead, comprising:
a bondable member formed from a portion of a bondable layer that comprises aluminum;
a barrier member formed from a portion of a barrier layer; wherein the barrier member disposed between the bondable member and the copper lead;
an auxiliary interconnect, comprising:
a second portion of the copper seed layer;
an auxiliary bonding cap coupled to the second portion of the copper seed layer, comprising:
an auxiliary member formed from a second portion of the bondable layer;
an auxiliary barrier member formed from a second portion of the barrier layer; and wherein the auxiliary barrier member disposed between the auxiliary bondable member and the second portion of the copper seed layer.

11. The device of Claim 10, wherein the bondable layer comprises sputtered aluminum and the barrier layer comprises sputtered titanium tungsten (TiW).

12. The device of Claim 10 or Claim 11, wherein the bondable layer comprises an aluminum alloy comprising silicon and copper.

13. The device of any of Claims 10 to 12, wherein the bondable layer comprises an aluminum alloy comprising between 1 percent silicon and between 0.5 and 2 percent copper.

14. The device of any of Claims 10 to 13, wherein the bondable layer comprises an aluminum alloy comprising about one (1) percent silicon and about one half (0.5) percent copper.

15. The device of any of Claims 10 to 14, wherein the barrier layer comprises titanium tungsten (TiW).

16. The device of any of Claims 10 to 15, wherein the portion of the copper seed layer electrically coupled to a portion of an underlying metal layer through a via in a dielectric layer; and
a portion of a second barrier layer is disposed between the portion of the copper seed layer and the portion of the underlying metal layer.

17. The device of Claim 16, wherein the second portion of the copper seed layer is electrically coupled to a second portion of the underlying metal layer through a second via in the dielectric layer; and
a second portion of the second barrier layer is disposed between the second portion of the copper seed layer and the second portion of the underlying metal layer.

18. The device of Claim 16 or Claim 17, wherein the second barrier layer comprises titanium tungsten (TiW).

19. The device of any of Claims 10 to 18, wherein the copper lead is formed to a thickness greater than 10,000 angstroms.

20. A combination layer mold, comprising:

a first cavity formed through a via in a layer of material;

the first cavity lined with a seed layer;

a second cavity formed in a photoresist layer; and

the second cavity disposed substantially over the first cavity.

21. The combination layer mold of Claim 20, further comprising a barrier layer disposed between the seed layer and the via.

22. The combination layer mold of Claim 20 or Claim 21, wherein the seed layer is a copper seed layer.

23. The combination layer mold of any of Claims 20 to 22, wherein the layer of material comprises a dielectric material.

24. The combination layer mold of any of Claims 20 to 23, further comprising the second cavity overlapping the first cavity.

25. The combination layer mold of any of Claims 20 to 24, further comprising the photoresist layer having a thickness greater than 10,000 angstroms.

26. The combination layer mold of any of Claims 20 to 25, further comprising the first cavity being formed through a plurality of vias in a plurality of layers of material.

27. An auxiliary interconnect, having a cap coupled to copper seed layer, comprising:

a bondable layer;

a barrier layer disposed between the bondable layer and the copper seed layer.

28. The interconnect of Claim 27, further comprising the seed layer being disposed on a second barrier layer.

29. The auxiliary interconnect of Claim 27 or Claim 28, wherein the bondable layer comprises sputtered aluminum and the barrier layer comprises sputtered titanium tungsten (TiW).

30. The auxiliary interconnect of any of Claims 27 to 29, wherein the bondable layer comprises an aluminum alloy comprising between 1 percent silicon and between 0.5 and 2 percent copper.

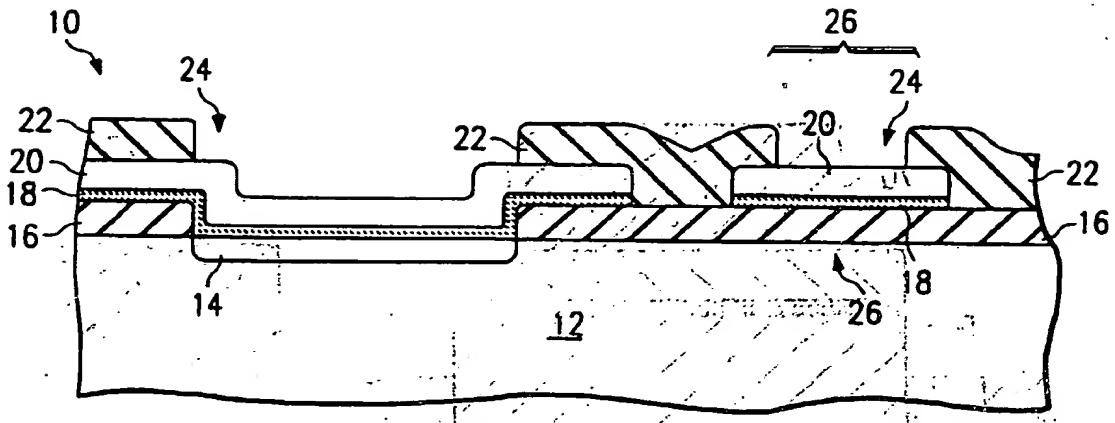

FIG. 1A

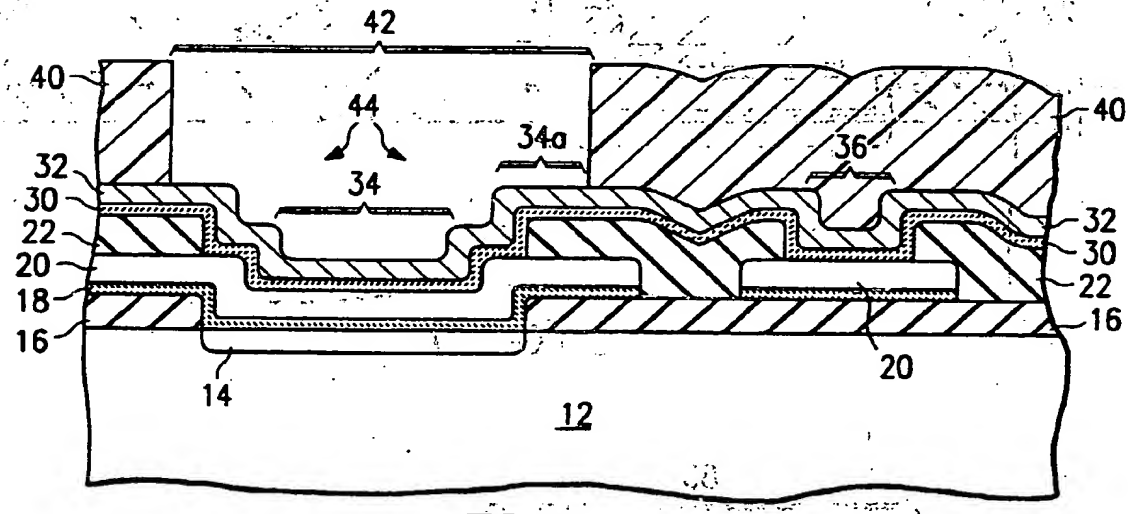

FIG. 1B

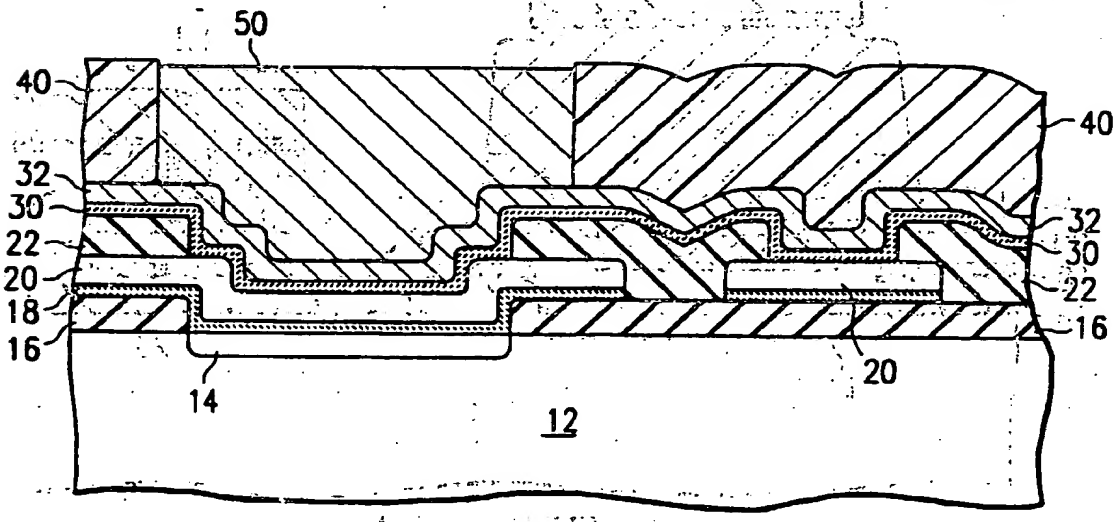

FIG. 1C

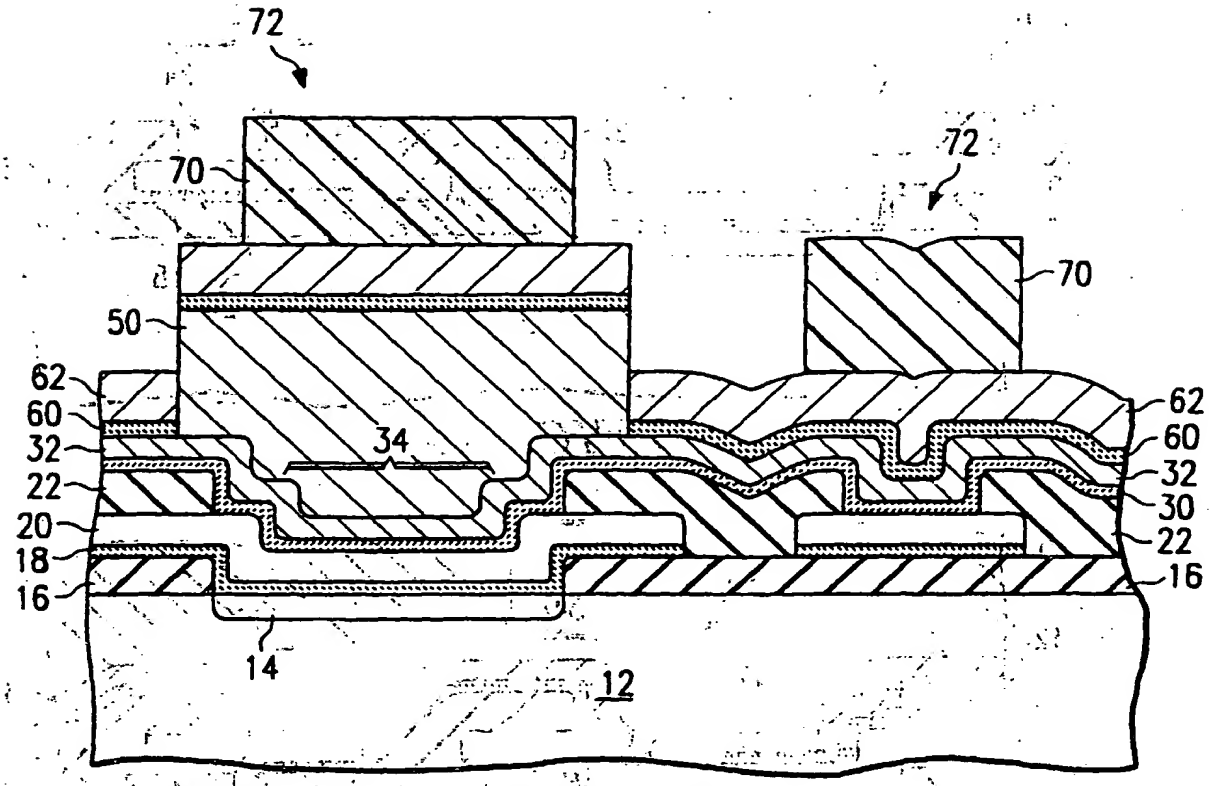
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FIG. 1D

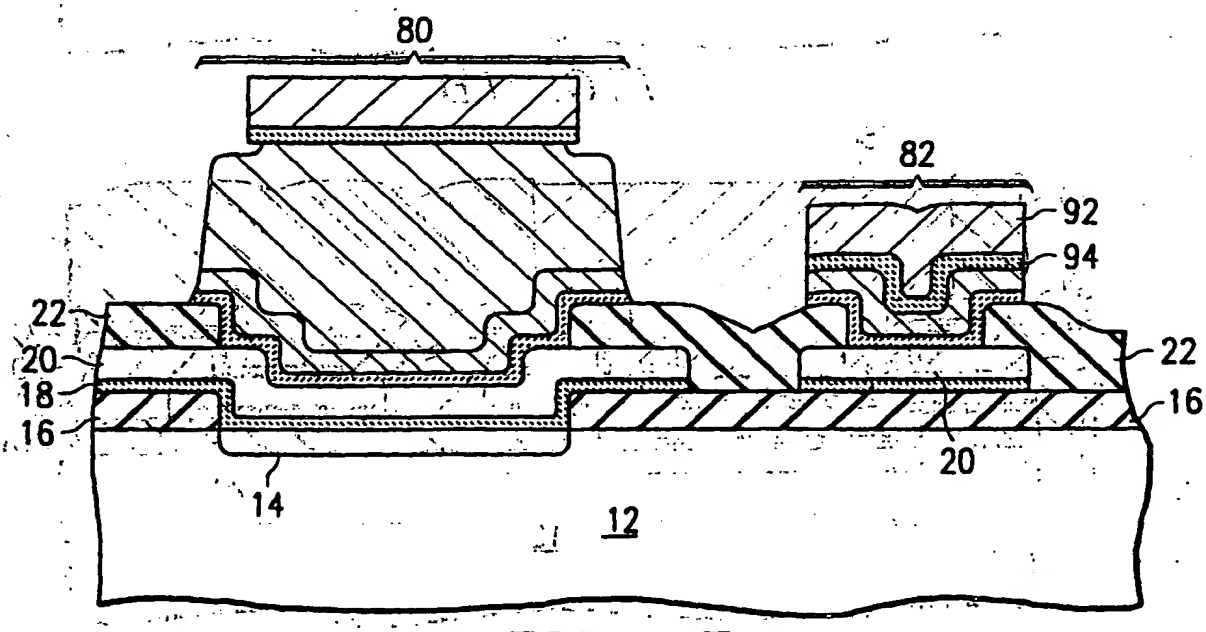
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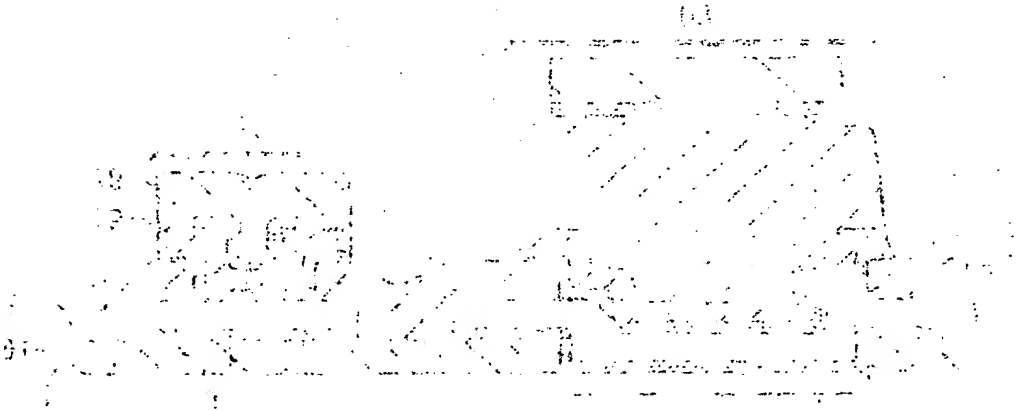
FIG. 1E



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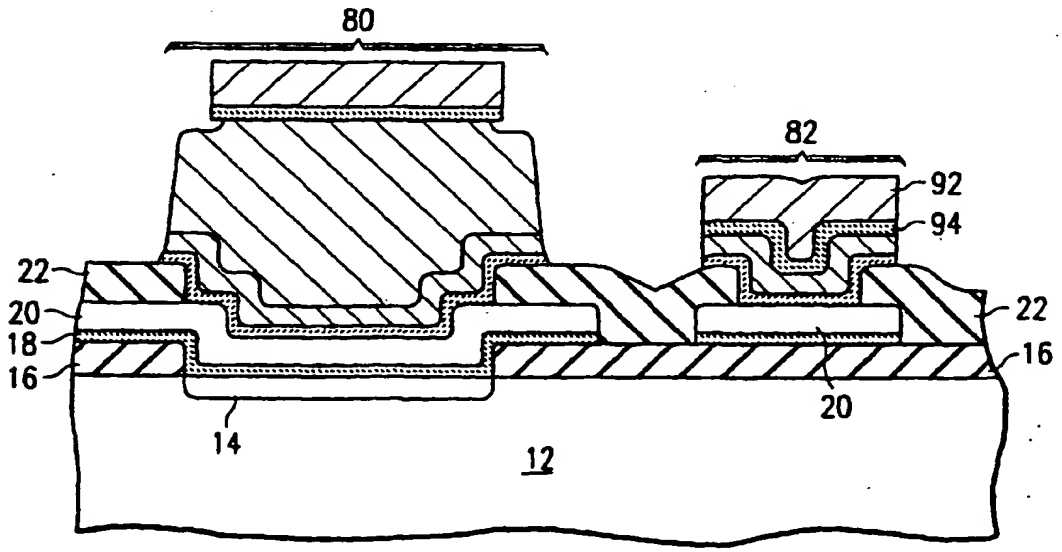

FIG. 1E

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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 31 0336

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X A	US 5 545 927 A (FAROOQ MUKTA S ET AL) 13 August 1996 (1996-08-13) * column 4, line 7 - column 6, line 11; figures 4-7 *	1,6-8, 27,28 10	H01L23/532
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TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	27 January 2000	Zeisler, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
O : non-written disclosure
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L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

Application Number
EP 97 31 0336

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☒ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☐ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

European Patent Office

LACK OF UNITY OF INVENTION
SHEET B

Application Number
EP 97 31 0336

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims: 1-19,27-30

   A plated interconnect having a bonding cap

2. Claims: 20-26

   A combination layer mold

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 97 31 0336

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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27-01-2000

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82